REMARKS

Applicants appreciate the detailed examination evidenced by the Official Action mailed September 27, 2004 (hereinafter the Official Action). Applicants also appreciate the allowance of Claims 1 – 8 and 25 – 41 as well as the Examiner's indication that Claims 10 – 15, 20, and 23 would be allowable if rewritten as outlined in the Official Action. *Official Action, page 4.* Applicants have amended claims 10 and 13 to be in independent form as suggested by the Examiner. Accordingly, Applicants respectfully submit that Claims 10 – 15 are in condition for allowance which is respectfully requested. Further, Applicants have rewritten Claims 20 and 23 to be in independent form as suggested by the Examiner. Accordingly, Claims 20 and 23 are also in condition for allowance, which is respectfully requested.

With regard to the remaining claims, Applicants have canceled several of the rejected claims and have amended Claim 19 to further highlight the patentable subject matter recited therein and to further distinguish the recited subject matter from the cited references as discussed below in greater detail. Applicants respectfully submit that the pending claims are patentable for at least the reasons discussed herein and respectfully request the allowance of all claims in due course.

Applicants respectfully request consideration of references cited in accompanying IDS

Applicants have submitted concurrently herewith a supplemental IDS including a reference cited in an Office Action for corresponding Korean Application Number 10-2002-0055290. The document listed on the attached PTO-1449 was first cited less than three months prior to the filing of the present supplemental IDS. Consideration of the cited references is respectfully requested.

Amended claim 19 is patentable over Lee and Kim.

Claims 9, 16, 18, 19, 21, and 24 stand rejected under 35 U.S.C. § 102 over U.S. Patent No. 5,699,306 to Lee et al. (hereinafter "Lee"). *Official Action, page 2.* As discussed briefly above, Applicants have canceled Claims 9 and 18 and have amended Claim 16 to depend from allowable Claim 10. Accordingly, Applicants remaining remark focus on the

patentability of Claims 19, 21 and 24 as these claims are the only remaining claims to which rejection under Lee is not moot.

Applicants have amended Claim 19 to recite in part:

> **a first redundancy circuit configured to store an address** of a defective memory cell in the memory device; and
> **a second redundancy circuit configured to store the address** of the defective memory cell, **wherein the address stored in the first redundancy circuit is accessed for a read operation to the defective memory cell in the memory and is not accessed for a write operation to the defective memory cell**.

As demonstrated by the above highlighted recitations of amended Claim 19, Lee does not disclose at least that "the address stored in the first redundancy circuit is accessed for a read operation to the defective memory cell and is not accessed for write operation to the defective memory cell." In particular, Lee appears to be directed to redundancy circuitry to replace defective redundant memory cells with other redundant memory cells. *Lee, column 2, lines 20 – 25.* In particular, Lee states that:

> The redundancy technique using electrical programming has an advantage in that the repair of defective normal memory cells is possible after completion of packaging. However, because redundant memory cells may also become defective, there remains a need for EEPROMs which are capable of repairing defective redundant memory cells as well after the completion of wafer processing and packaging.
>
> **Prior EEPROMs have never been able to determine whether defects exist in redundant memory cells prior to the replacement of normal memory cells therewith. Therefore, the possibility of defects still remains after the replacement. Accordingly, there is a need for EEPROMS that are capable of selecting redundant memory cells and then determining the presence or absence of their defects**
>
> **Furthermore, after replacing defective normal memory cells with redundant memory cells by laser programming, any one of the replacement redundant memory cells may later develop a defect. In this case, different redundant memory cells can be used as replacements by electrically programming the same address used when first specifying the defective normal memory cells. However, subsequent reception of the specified address causes the first and second redundant memory cells to be selected at the same time, resulting in a malfunction.**

Lee, column 1, lines 37 – 67 and column 2, lines 1 – 9 (Emphasis added).

As demonstrated by the above cited passage of Lee, the problem addressed therein focuses on the situation where the redundant memory cells intended to replace defective cells are themselves determined to be defective. Going further, Lee specifies that it was possible to replace faulty redundant cells with different redundant memory cells by electrically programming the same address used to specify the defective normal memory cell. Lee goes on to point out that the problem with this type of approach is that "the specified address causes the first and second redundant memory cells to be selected at the same time, resulting in a malfunction." *Lee, column 2, lines 7 – 10.* Therefore, as understood by Applicants, the above approach outlined by Lee indicates that the first and second redundant memory cells would be selected without regard to which type of memory access is used. In other words, Lee appears to indicate that both the first and second redundant memory cells are selected regardless of the type of memory cycle requested. Accordingly, Applicants respectfully submit that Lee does not disclose at least that "the address stored in the first redundancy circuits is accessed for a read operation to the defective memory cell in the memory and is not accessed for a write operation to the defective memory cell" as recited in amended Claim 19. Accordingly, Claim 19 is patentable over Lee for at least these reasons. Furthermore, Claims 21 and 24 have both been amended to depend from Claim 19 and are therefore patentable at least per the patentability of Claim 19 as discussed above. Accordingly, Applicants respectfully request the withdrawal of the rejections to these claims under Lee and the allowance thereof.

Amended Claim 19 is patentable over Kim.

Claims 9, 16, 18, 19, 21, and 24 stand rejected under 25 U.S.C. § 102 over U.S. Patent No. 6,462,994 to Kim ("Kim"). *Official Action, page 3.* As discussed above, Applicants have canceled Claims 9 and 18 and have further amended Claim 16 to depend from allowable Claim 10. Accordingly, Applicants remaining remarks focus solely on the recitations of Claim 19, 21, and 24, which as understood by Applicants are the only pending claims for which the rejection under Kim is not moot.

As discussed above, Claim 19 has been amended to recite in-part:

> **a first redundancy circuit configured to store an address of a defective memory cell** in the memory device; and

> **a second redundancy circuit configured to store the address of the defective memory cell,** wherein the address stored in the first redundancy circuit is accessed for a read operation to the defective memory cell in the memory and is not accessed for a write operation to the defective memory cell.

As demonstrated by the above highlighted recitations of amended Claim 19, Kim does not disclose at least a first redundancy circuit configured to store the address of a defective memory cell and a second redundancy circuit configured to store the address of the defective memory cell. In particular, the passage of Kim relied on by the Official Action appears to be the recitations of Claim 15 therein which read (with emphasis added):

> an address buffer for receiving an external address;
> a row decoder for decoding a row address provided by the address buffer, and generating a word line selecting signal;
> a column decoder for decoding a column address provided by the address buffer, and generating a bit line selecting signal;
> a memory cell array having a plurality of memory cells, each of the plurality of memory cells being activated by a selection of a word line and a bit line by the word line selecting signal and the bit line selecting signal, respectively;
> **first redundancy logic cells for replacing defect cells;**
> **second redundancy logic cells for replacing the defect cells;**
> **a plurality of defect cell address latches for storing defect cell addresses corresponding to the defect cells, the defect cells being detected in a test mode;**
> a plurality of comparators for outputting repair signals when an address stored in the plurality of defect cell address latches corresponds to the external address received from the address buffer; and
> a redundancy controller for generating a control signal to intercept a pass of defect cell address signals of the row decoder and the column decoder in response to the repair signal, generating a first control signal to enable a read/write operation of the first redundancy logic cell when the memory cell array has the defect cells, and generating a second control signal to enable a read/write operation of the second redundancy logic cell when the first redundancy logic cell has the defect cells, the generating of the control signal, the first control signal, and the second control signal occurring in a normal mode.

As demonstrated by the above highlighted recitations of Claim 15 in Kim, the Official Action appears to consider the recitations of first and second redundancy logic cells therein to disclose the first and second redundancy circuits recited in amended Claim 19. However,

Applicants respectfully point out that the first and second redundancy circuits recited in Claim 19 are configured to store an address of a defective memory cell. In contrast, the first and second redundancy logic cells relied on by the Official Action are apparently not configured to store addresses. In fact, the first and second redundancy logic cells of Kim are discussed in reference to Figure 1 as follows: "the enable-signal activates the redundancy logic cell 28 to read data stored in a data-bus by a read-control signal R, or to write data from a data-bus by a write-control signal W." *Kim, column 4, line 67, column 5, lines 1 –3.* As understood by Applicants, the above-cited passage of Kim demonstrates that the redundancy logic cells 28 in Kim actually store **data**, not an **address** as recited in Claim 19. Moreover, Kim discusses other circuitry (defective-cell-address latch unit 22) which is described as follows: "[t]he defective-cell-address latch unit 22 comprises many latches. The defective-cell-address latch unit 22 latches a defect cell address when a package test finds a malfunctioned cell among the memory cell array 16 and among [sic] repaired cells." *Kim, column 4, lines 51 – 55.* Therefore, as understood by Applicants, it is the defective cell address latch units in Kim that store addresses, not the redundancy logic cells 28. Moreover, the defective cell address latch units are not disclosed to include a first redundancy circuit configured to store an address of a defective memory cell and a second redundancy circuit configured to store the address of a defective memory cell as recited in amended Claim 19. In addition, the defective cell address latch units of Kim are also not disclosed to be configured so that a first one of the defective cell address latch unit 22 is accessed for a read operation but not accessed for a write operation as further recited in amended Claim 19. Accordingly, Claim 19 is patentable over Kim for at least the reasons discussed above. Furthermore, dependent Claims 21 and 24 are also patentable for at least the patentability of Claim 19 as discussed above.

Claim 22 is patentable over Lee, Kim in view of Akaogi.

Claims 17 and 22 stand rejected 35 U.S.C.§ 103 over Lee/Kim in view of U.S. Patent No. 6,240,040 to Akaogi et al. ("Akaogi") *Official Action, page 3.* As discussed above, Claim 17 has been amended to depend from allowable Claim 10. Accordingly, the rejection of Claim 17 over Lee/Kim and Akaogi is now moot and should be withdrawn.

With respect to Claim 22, as discussed above, Lee and Kim do not disclose at least the recitations discussed above in reference to Claim 19. Accordingly, even if Lee and Kim were combined as alleged, the combination would not teach all of the recitations of Claim 22 as this claim includes all the recitations of Claim 19 which, as discussed above, is patentable over Lee and Kim. Accordingly, Claim 22 is patentable over Lee/Kim in view of Akaogi for at least these reasons.

CONCLUSION

Applicants have placed several of the indicated allowable claims in condition for allowance as suggested by the Examiner. Applicants have canceled numerous rejected claims while rewriting others in allowable form. Applicants also amended Claim 19 to further highlight the patentable recitations therein and have shown at least some of the distinction between Lee and Kim. Accordingly, Applicants respectfully submit that all claims are in condition for allowance which is respectfully requested in due course. If any informal matters arise, the Examiner is encouraged to contact the undersigned by telephone at (919) 854-1400.

Respectfully submitted,

Robert N. Crouse
Registration No. 44,635

USPTO Customer No. 20792
Myers Bigel Sibley & Sajovec
Post Office Box 37428
Raleigh, North Carolina 27627
Telephone: 919/854-1400
Facsimile: 919/854-1401

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Candi L. Riggs